

## 74VCX32374

### Low Voltage 32-Bit D-Type Flip-Flops with 3.6V Tolerant Inputs and Outputs

#### General Description

The VCX32374 contains thirty-two non-inverting D-type flip-flops with 3-STATE outputs and is intended for bus oriented applications. The device is byte controlled. A buffered clock (CP) and output enable ( $\overline{OE}$ ) are common to each byte and can be shorted together for full 32-bit operation.

The 74VCX32374 is designed for low voltage (1.2V to 3.6V)  $V_{CC}$  applications with I/O compatibility up to 3.6V.

The 74VCX32374 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining low CMOS power dissipation.

#### Features

- 1.2V to 3.6V  $V_{CC}$  supply operation
- 3.6V tolerant inputs and outputs
- $t_{PD}$ 
  - 3.0 ns max for 3.0V to 3.6V  $V_{CC}$
- Power-off high impedance inputs and outputs
- Supports live insertion and withdrawal (Note 1)
- Static Drive ( $I_{OH}/I_{OL}$ )
  - $\pm 24$  mA @ 3.0V  $V_{CC}$
- Uses patented noise/EMI reduction circuitry
- Latch-up performance exceeds 300 mA
- ESD performance:
  - Human body model > 2000V
  - Machine model > 200V
- Packaged in plastic Fine-Pitch Ball Grid Array (FBGA)

**Note 1:** To ensure the high-impedance state during power up or power down, OE should be tied to  $V_{CC}$  through a pull-up resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

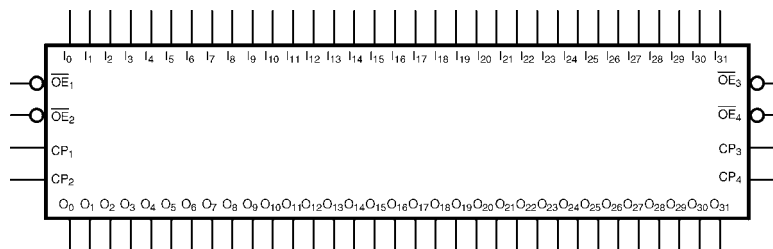
#### Ordering Code:

Order Number	Package Number	Package Descriptions
74VCX32374G (Note 2)(Note 3)	BGA96A	96-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide

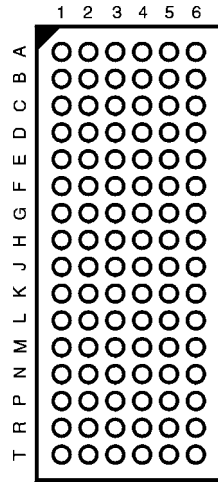
**Note 2:** Ordering code "G" indicates Trays.

**Note 3:** Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

#### Logic Symbol



### Connection Diagram



(Top Thru View)

### Pin Descriptions

Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active LOW)
$CP_n$	Clock Pulse Input
$I_0-I_{31}$	Inputs
$O_0-O_{31}$	Outputs

### FBGA Pin Assignments

	1	2	3	4	5	6
<b>A</b>	$O_1$	$O_0$	$\overline{OE}_1$	$CP_1$	$I_0$	$I_1$
<b>B</b>	$O_3$	$O_2$	GND	GND	$I_2$	$I_3$
<b>C</b>	$O_5$	$O_4$	$V_{CC}$	$V_{CC}$	$I_4$	$I_5$
<b>D</b>	$O_7$	$O_6$	GND	GND	$I_6$	$I_7$
<b>E</b>	$O_9$	$O_8$	GND	GND	$I_8$	$I_9$
<b>F</b>	$O_{11}$	$O_{10}$	$V_{CC}$	$V_{CC}$	$I_{10}$	$I_{11}$
<b>G</b>	$O_{13}$	$O_{12}$	GND	GND	$I_{12}$	$I_{13}$
<b>H</b>	$O_{14}$	$O_{15}$	$\overline{OE}_2$	$CP_2$	$I_{15}$	$I_{14}$
<b>J</b>	$O_{17}$	$O_{16}$	$\overline{OE}_3$	$CP_3$	$I_{16}$	$I_{17}$
<b>K</b>	$O_{19}$	$O_{18}$	GND	GND	$I_{18}$	$I_{19}$
<b>L</b>	$O_{21}$	$O_{20}$	$V_{CC}$	$V_{CC}$	$I_{20}$	$I_{21}$
<b>M</b>	$O_{23}$	$O_{22}$	GND	GND	$I_{22}$	$I_{23}$
<b>N</b>	$O_{25}$	$O_{24}$	GND	GND	$I_{24}$	$I_{25}$
<b>P</b>	$O_{27}$	$O_{26}$	$V_{CC}$	$V_{CC}$	$I_{26}$	$I_{27}$
<b>R</b>	$O_{29}$	$O_{28}$	GND	GND	$I_{28}$	$I_{29}$
<b>T</b>	$O_{30}$	$O_{31}$	$\overline{OE}_4$	$CP_4$	$I_{31}$	$I_{30}$

### Truth Tables

Inputs			Outputs
$CP_1$	$\overline{OE}_1$	$I_0-I_7$	$O_0-O_7$
↗	L	H	H
↗	L	L	L
L	L	X	$O_0$
X	H	X	Z

Inputs			Outputs
$CP_2$	$\overline{OE}_2$	$I_8-I_{15}$	$O_8-O_{15}$
↗	L	H	H
↗	L	L	L
L	L	X	$O_0$
X	H	X	Z

Inputs			Outputs
$CP_3$	$\overline{OE}_3$	$I_{16}-I_{23}$	$O_{16}-O_{23}$
↗	L	H	H
↗	L	L	L
L	L	X	$O_0$
X	H	X	Z

Inputs			Outputs
$CP_4$	$\overline{OE}_4$	$I_{24}-I_{31}$	$O_{24}-O_{31}$
↗	L	H	H
↗	L	L	L
L	L	X	$O_0$
X	H	X	Z

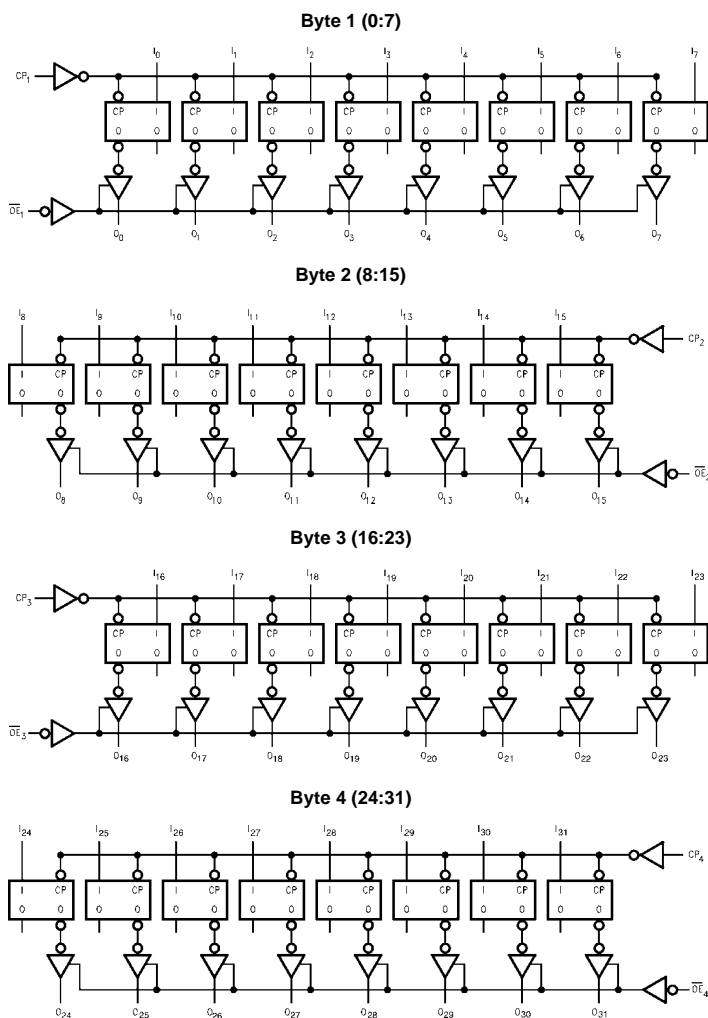
H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial (HIGH or LOW, inputs may not float)  
 Z = High Impedance  
 $O_0$  = Previous  $O_0$  before HIGH-to-LOW of CP

## Functional Description

The 74VCX32374 consists of thirty-two edge-triggered flip-flops with individual D-type inputs and 3-STATE true outputs. The device is byte controlled with each byte functioning identically, but independent of the other. The control pins can be shorted together to obtain full 32-bit operation. Each clock has a buffered clock and buffered Output Enable common to all flip-flops within that byte. The description which follows applies to each byte. Each

flip-flop will store the state of their individual I inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock ( $CP_n$ ) transition. With the Output Enable ( $\overline{OE}_n$ ) LOW, the contents of the flip-flops are available at the outputs. When  $\overline{OE}_n$  is HIGH, the outputs go to the high impedance state. Operations of the  $\overline{OE}_n$  input does not affect the state of the flip-flops.

## Logic Diagrams



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

**Absolute Maximum Ratings** (Note 4)

Supply Voltage ( $V_{CC}$ )	-0.5V to +4.6V
DC Input Voltage ( $V_I$ )	-0.5V to +4.6V
Output Voltage ( $V_O$ )	
Outputs 3-STATED	-0.5V to +4.6V
Outputs Active (Note 5)	-0.5V to $V_{CC} + 0.5V$
DC Input Diode Current ( $I_{IK}$ ) $V_I < 0V$	-50 mA
DC Output Diode Current ( $I_{OK}$ )	
$V_O < 0V$	-50 mA
$V_O > V_{CC}$	+50 mA
DC Output Source/Sink Current	
( $I_{OH}/I_{OL}$ )	$\pm 50$ mA
DC $V_{CC}$ or GND Current per	
Supply Pin ( $I_{CC}$ or GND)	$\pm 100$ mA
Storage Temperature Range ( $T_{STG}$ )	-65°C to +150°C

**Recommended Operating Conditions** (Note 6)

Power Supply	
Operating	1.2V to 3.6V
Input Voltage	-0.3V to +3.6V
Output Voltage ( $V_O$ )	
Output in Active States	0V to $V_{CC}$
Output in 3-STATE	0.0V to 3.6V
Output Current in $I_{OH}/I_{OL}$	
$V_{CC} = 3.0V$ to 3.6V	$\pm 24$ mA
$V_{CC} = 2.3V$ to 2.7V	$\pm 18$ mA
$V_{CC} = 1.65V$ to 2.3V	$\pm 6$ mA
$V_{CC} = 1.4V$ to 1.6V	$\pm 2$ mA
$V_{CC} = 1.2V$	$\pm 100$ $\mu A$
Free Air Operating Temperature ( $T_A$ )	-40°C to +85°C
Minimum Input Edge Rate ( $\Delta t/\Delta V$ )	
$V_{IN} = 0.8V$ to 2.0V, $V_{CC} = 3.0V$	10 ns/V

**Note 4:** The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Note 5:**  $I_O$  Absolute Maximum Rating must be observed.

**Note 6:** Floating or unused inputs must be held HIGH or LOW.

**DC Electrical Characteristics**

Symbol	Parameter	Conditions	$V_{CC}$ (V)	Min	Max	Units
$V_{IH}$	HIGH Level Input Voltage		2.7 - 3.6	2.0		V
			2.3 - 2.7	1.6		
			1.65 - 2.3	$0.65 \times V_{CC}$		
			1.4 - 1.6	$0.65 \times V_{CC}$		
			1.2	$0.65 \times V_{CC}$		
$V_{IL}$	LOW Level Input Voltage		2.7 - 3.6		0.8	V
			2.3 - 2.7		0.7	
			1.65 - 2.3		$0.35 \times V_{CC}$	
			1.4 - 1.6		$0.35 \times V_{CC}$	
			1.2		$0.05 \times V_{CC}$	
$V_{OH}$	HIGH Level Output Voltage	$I_{OH} = -100 \mu A$ $I_{OH} = -12$ mA $I_{OH} = -18$ mA $I_{OH} = -24$ mA	2.7 - 3.6	$V_{CC} - 0.2$		V
			2.7	2.2		
			3.0	2.4		
			3.0	2.2		
		$I_{OH} = -100 \mu A$ $I_{OH} = -6$ mA $I_{OH} = -12$ mA $I_{OH} = -18$ mA	2.3 - 2.7	$V_{CC} - 0.2$		
			2.3	2.0		
			2.3	1.8		
			2.3	1.7		
		$I_{OH} = -100 \mu A$ $I_{OH} = -6$ mA	1.65 - 2.3	$V_{CC} - 0.2$		
			1.65	1.25		
		$I_{OH} = -100 \mu A$ $I_{OH} = -2$ mA	1.4 - 1.6	$V_{CC} - 0.2$		
			1.4	1.05		
		$I_{OH} = -100 \mu A$	1.2	$V_{CC} - 0.2$		

**DC Electrical Characteristics** (Continued)

Symbol	Parameter	Conditions	V <sub>CC</sub> (V)	Min	Max	Units
V <sub>OL</sub>	LOW Level Output Voltage	I <sub>OL</sub> = 100 μA	2.7 - 3.6		0.2	V
		I <sub>OL</sub> = 12 mA	2.7		0.4	
		I <sub>OL</sub> = 18 mA	3.0		0.4	
		I <sub>OL</sub> = 24 mA	3.0		0.55	
		I <sub>OL</sub> = 100 μA	2.7 - 2.7		0.2	
		I <sub>OL</sub> = 12 mA	2.3		0.4	
		I <sub>OL</sub> = 18 mA	2.3		0.6	
		I <sub>OL</sub> = 100 μA	1.65 - 2.3		0.2	
		I <sub>OL</sub> = 6 mA	1.65		0.3	
		I <sub>OL</sub> = 100 μA	1.4 - 1.6		0.2	
I <sub>OL</sub> = 2 mA	1.4		0.35			
I <sub>OL</sub> = 100 μA	1.2		0.05			
I <sub>I</sub>	Input Leakage Current	0 ≤ V <sub>I</sub> ≤ 3.6V	1.2 - 3.6		±5.0	μA
I <sub>OZ</sub>	3-STATE Output Leakage	0 ≤ V <sub>O</sub> ≤ 3.6V V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	1.2 - 3.6		±10	μA
I <sub>OFF</sub>	Power-OFF Leakage Current	0 ≤ (V <sub>I</sub> , V <sub>O</sub> ) ≤ 3.6V	0		10	μA
I <sub>CC</sub>	Quiescent Supply Current	V <sub>I</sub> = V <sub>CC</sub> or GND	1.2 - 3.6		40	μA
		V <sub>CC</sub> ≤ (V <sub>I</sub> , V <sub>O</sub> ) ≤ 3.6V (Note 7)	1.2 - 3.6		±40	μA
ΔI <sub>CC</sub>	Increase in I <sub>CC</sub> per Input	V <sub>IH</sub> = V <sub>CC</sub> - 0.6V	2.7 - 3.6		750	μA

**Note 7:** Outputs disabled or 3-STATE only.**AC Electrical Characteristics** (Note 8)

Symbol	Parameter	Conditions	V <sub>CC</sub> (V)	T <sub>A</sub> = -40°C to +85°C		Units	Figure Number	
				Min	Max			
f <sub>MAX</sub>	Maximum Clock Frequency Setup Time	C <sub>L</sub> = 30 pF, R <sub>L</sub> = 500Ω	3.3 ± 0.3	250		MHz		
			2.5 ± 0.2	200				
			1.8 ± 0.15	100				
		C <sub>L</sub> = 15 pF, R <sub>L</sub> = 2kΩ		1.5 ± 0.1	80			
				1.2	40			
t <sub>PHL</sub> , t <sub>PLH</sub>	Propagation Delay	C <sub>L</sub> = 30 pF, R <sub>L</sub> = 500Ω	3.3 ± 0.3	0.8	3.0	ns	Figures 1, 2	
			2.5 ± 0.2	1.0	3.9			
			1.8 ± 0.15	1.5	7.8			
		C <sub>L</sub> = 15 pF, R <sub>L</sub> = 2kΩ		1.5 ± 0.1	1.0			15.6
				1.2	1.5			39
t <sub>PZL</sub> , t <sub>PZH</sub>	Output Enable Time	C <sub>L</sub> = 30 pF, R <sub>L</sub> = 500Ω	3.3 ± 0.3	0.8	3.5	ns	Figures 1, 3, 4	
			2.5 ± 0.2	1.0	4.6			
			1.8 ± 0.15	1.5	9.2			
		C <sub>L</sub> = 15 pF, R <sub>L</sub> = 2kΩ		1.5 ± 0.1	1.0			18.4
				1.2	1.5			46
t <sub>PLZ</sub> , t <sub>PHZ</sub>	Output Disable Time	C <sub>L</sub> = 30 pF, R <sub>L</sub> = 500Ω	3.3 ± 0.3	0.8	3.5	ns	Figures 1, 3, 4	
			2.5 ± 0.2	1.0	3.8			
			1.8 ± 0.15	1.5	6.8			
		C <sub>L</sub> = 15 pF, R <sub>L</sub> = 2kΩ		1.5 ± 0.1	1.0			13.6
				1.2	1.5			34
t <sub>S</sub>	Setup Time	C <sub>L</sub> = 30 pF, R <sub>L</sub> = 500Ω	3.3 ± 0.3	1.5		ns	Figures 1, 6	
			2.5 ± 0.2	1.5				
			1.8 ± 0.15	2.5				
		C <sub>L</sub> = 15 pF, R <sub>L</sub> = 500Ω		1.5 ± 0.1	3			
				1.2	6			

## AC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	V <sub>CC</sub> (V)	T <sub>A</sub> = -40°C to +85°C		Units	Figure Number
				Min	Max		
t <sub>H</sub>	Hold Time	C <sub>L</sub> = 30 pF, R <sub>L</sub> = 500Ω	3.3 ± 0.3	1.0		ns	Figures 1, 6
			2.5 ± 0.2	1.0			
			1.8 ± 0.15	1.0			
		C <sub>L</sub> = 15 pF, R <sub>L</sub> = 500Ω	1.5 ± 0.1	2.0			Figures 6, 7
			1.2	6			
t <sub>W</sub>	Pulse Width	C <sub>L</sub> = 30 pF, R <sub>L</sub> = 500Ω	3.3 ± 0.3	1.5		ns	Figures 1, 5
			2.5 ± 0.2	1.5			
			1.8 ± 0.15	4.0			
		C <sub>L</sub> = 15 pF, R <sub>L</sub> = 500Ω	1.5 ± 0.1	4.0			Figures 5, 7
			1.2	8			

**Note 8:** For C<sub>L</sub> = 50pF, add approximately 300 ps to the AC maximum specification.

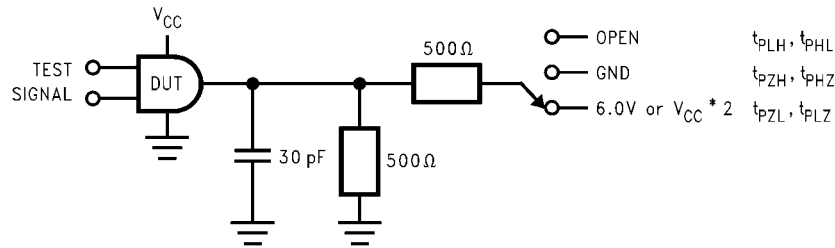
## Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V <sub>CC</sub> (V)	T <sub>A</sub> = +25°C	Units
				Typical	
V <sub>OLP</sub>	Quiet Output Dynamic Peak V <sub>OL</sub>	C <sub>L</sub> = 30 pF, V <sub>IH</sub> = V <sub>CC</sub> , V <sub>IL</sub> = 0V	1.8	0.25	V
			2.5	0.6	
			3.3	0.8	
V <sub>OLV</sub>	Quiet Output Dynamic Valley V <sub>OL</sub>	C <sub>L</sub> = 30 pF, V <sub>IH</sub> = V <sub>CC</sub> , V <sub>IL</sub> = 0V	1.8	-0.25	V
			2.5	-0.6	
			3.3	-0.8	
V <sub>OHV</sub>	Quiet Output Dynamic Valley V <sub>OH</sub>	C <sub>L</sub> = 30 pF, V <sub>IH</sub> = V <sub>CC</sub> , V <sub>IL</sub> = 0V	1.8	1.5	V
			2.5	1.9	
			3.3	2.2	

## Capacitance

Symbol	Parameter	Conditions	T <sub>A</sub> = +25°C	Units
			Typical	
C <sub>IN</sub>	Input Capacitance	V <sub>CC</sub> = 1.8V, 2.5V or 3.3V, V <sub>I</sub> = 0V or V <sub>CC</sub>	6	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>I</sub> = 0V or V <sub>CC</sub> , V <sub>CC</sub> = 1.8V, 2.5V or 3.3V	7	pF
C <sub>PD</sub>	Power Dissipation Capacitance	V <sub>I</sub> = 0V or V <sub>CC</sub> , f = 10 MHz, V <sub>CC</sub> = 1.8V, 2.5V or 3.3V	20	pF

**AC Loading and Waveforms ( $V_{CC}$  3.3V ± 0.3V to 1.8V ± 0.15V)**



TEST	SWITCH
$t_{PLH}, t_{PHL}$	Open
$t_{PZL}, t_{PLZ}$	6V at $V_{CC} = 3.3V \pm 0.3V$ ; $V_{CC} \times 2V$ at $V_{CC} = 2.5V \pm 0.2V; 1.8V \pm 0.15V$
$t_{PZH}, t_{PHZ}$	GND

FIGURE 1. AC Test Circuit

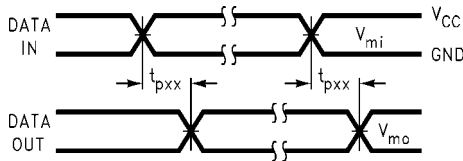


FIGURE 2. Waveform for Inverting and Non-Inverting Functions

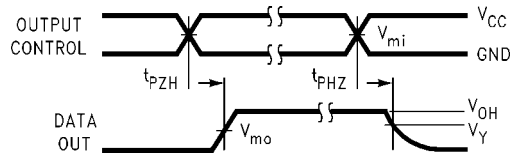


FIGURE 3. 3-STATE Output High Enable and Disable Times for Low Voltage Logic

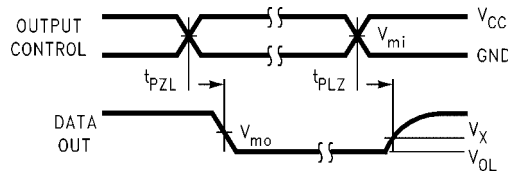


FIGURE 4. 3-STATE Output Low Enable and Disable Times for Low Voltage Logic

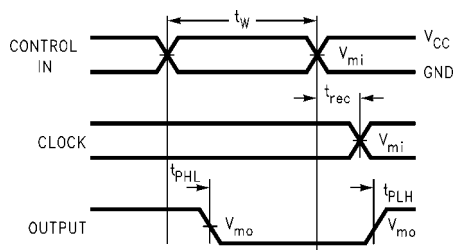


FIGURE 5. Propagation Delay, Pulse Width and  $t_{rec}$  Waveforms

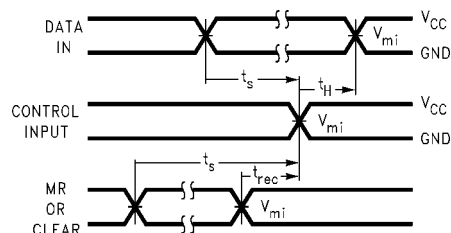
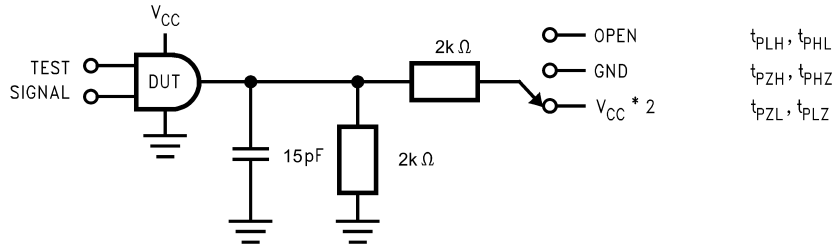


FIGURE 6. Setup Time, Hold Time and Recovery Time for Low Voltage Logic

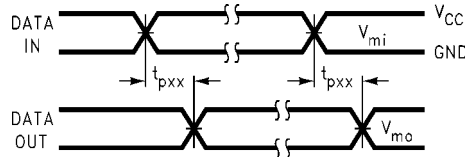
Symbol	$V_{CC}$		
	3.3V ± 0.3V	2.5V ± 0.2V	1.8V ± 0.15V
$V_{mi}$	1.5V	$V_{CC}/2$	$V_{CC}/2$
$V_{mo}$	1.5V	$V_{CC}/2$	$V_{CC}/2$
$V_X$	$V_{OL} + 0.3V$	$V_{OL} + 0.15V$	$V_{OL} + 0.15V$
$V_Y$	$V_{OH} - 0.3V$	$V_{OH} - 0.15V$	$V_{OH} - 0.15V$

**AC Loading and Waveforms ( $V_{CC}$  1.5V ± 0.1V to 1.2V)**

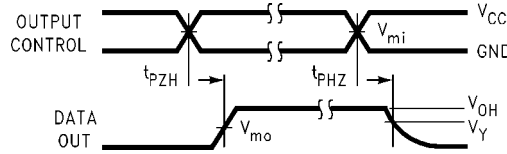


TEST	SWITCH
$t_{PLH}, t_{PHL}$	Open
$t_{PZL}, t_{PLZ}$	$V_{CC} \times 2V$ at $V_{CC} = 1.5V \pm 0.1V$
$t_{PZH}, t_{PHZ}$	GND

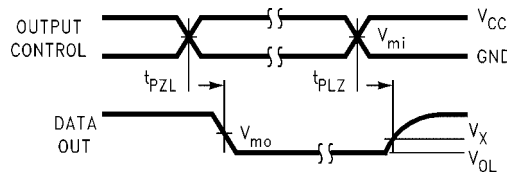
**FIGURE 7. AC Test Circuit**



**FIGURE 8. Waveform for Inverting and Non-Inverting Functions**



**FIGURE 9. 3-STATE Output High Enable and Disable Times for Low Voltage Logic**

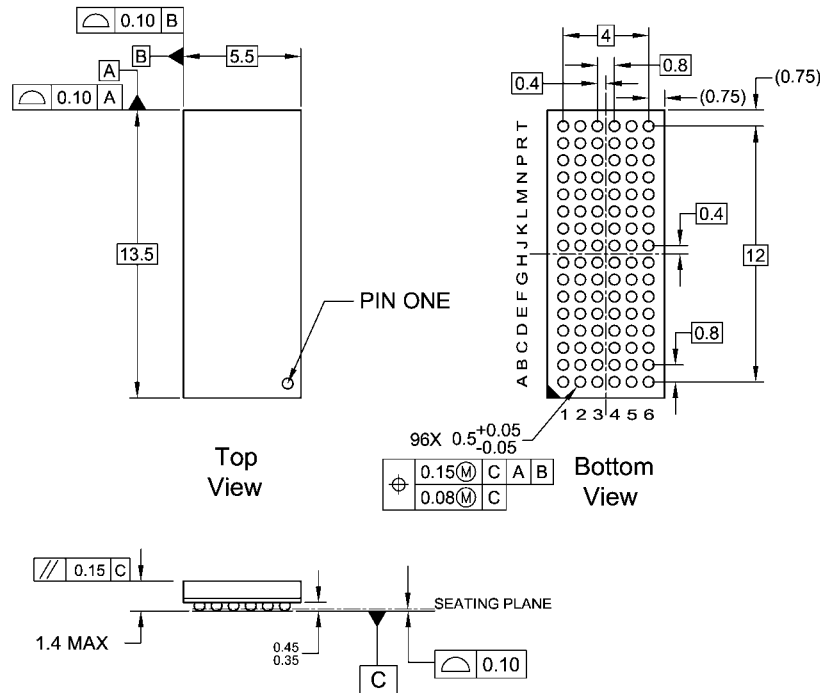


**FIGURE 10. 3-STATE Output Low Enable and Disable Times for Low Voltage Logic**

Symbol	$V_{CC}$
	1.5V ± 0.1V
$V_{mi}$	$V_{CC}/2$
$V_{mo}$	$V_{CC}/2$
$V_X$	$V_{OL} + 0.1V$
$V_Y$	$V_{OH} - 0.1V$



**Physical Dimensions** inches (millimeters) unless otherwise noted



**NOTES:**

- A. THIS PACKAGE CONFORMS TO JEDEC M0-205
- B. ALL DIMENSIONS IN MILLIMETERS
- C. LAND PATTERN RECOMMENDATION: NSMD (Non Solder Mask Defined)  
.35MM DIA PADS WITH A SOLDERMASK OPENING OF .45MM CONCENTRIC TO PADS
- D. DRAWING CONFORMS TO ASME Y14.5M-1994

BGA96ArevE

**96-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC M0-205, 5.5mm Wide  
Package Number BGA96A**

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**LIFE SUPPORT POLICY**

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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